REMARKS

Claims 5-12 were previously pending in this application. Claims 1-4 stand withdrawn as non-elected and are hereby cancelled without prejudice for presentation in a divisional application.

Claims 5-8, and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,380,084 issued Linn et al. ("Linn").

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Linn as applied to claim 5 above, and furthering view of U.S. Patent No. 5,801,096 issued to Lee et al.("Lee").

Claim 1 is amended.

New claims 13-15 are added.

No new matter is added.

With entry of this amendment, claims 5-15 remain in the case for reconsideration.

Reconsideration is respectfully requested.

Claim Rejections – 35 USC § 102

Claims 5-8, and 10-12 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Linn.

The rejection is respectfully traversed.

Claim 5 is amended to recite:

"forming a contact plug in the contact hole by forming a first sub-plug that fills a lower portion of the contact hole and forming a second sub-plug that fills an upper portion of the contact hole on the first sub-plug,

wherein the first sub-plug fills a lower portion of the contact hole to a level substantially below a top surface of the insulating layer."

The Examiner alleges that Linn teaches:

"forming an insulating layer (52) having a contact hole therethrough on a semiconductor substrate (40)...

forming a plug in the contact hole...."

On the contrary, Linn merely teaches forming copper vias, not a contact plug as recited in amended claim 5. The copper vias are formed by filling the openings or via trenches formed in the intermetal dielectric layers (the dielectric layers between metal levels) with copper according to the Linn reference. And via caps 68 merely overlie the vias for

encapsulation. See FIGS. 15-16 of the Linn reference. Also see S. Wolf, Silicon Processing for the VLSI Era Volume 2 – Process Integration 189 (1990).

The specification of the present application at page 1, lines 12-22, however, explains the contact plug as follows:

A contact plug formed within an insulating layer between a semiconductor substrate and a bit line or a storage electrode has been used for connecting an active region on the semiconductor substrate and the bit line, for connecting an active region on a semiconductor substrate and a storage electrode of a capacitor, and for connecting an active region of a peripheral circuit or a gate electrode and a bit line.

For this reason, vias of the Linn reference are different from a contact plug as recited in claim 5. Linn, therefore, does not teach or disclose forming a contact plug in a contact hole.

Further, the Linn reference does not teach or disclose "the first sub-plug fills a lower portion of the contact hole to a level substantially below a top surface of the insulating layer, as further recited in amended claim 5.

Accordingly, Linn does not teach or disclose all of the elements of claim 5 and, thus, does not anticipate claim 5, especially in view of the amendment. Also, claims 6-12, which depend from allowable claim 5 and recite features that are neither disclosed or taught by the Linn reference, are allowable.

Additionally, the Linn reference does not teach features of new claims 13-15, such as "the plug formed in the contact hole contacts a surface of the semiconductor substrate" as recited in claim 13. Accordingly, new claims 13-15 are also allowable.

Claim Rejections – 35 USC § 103

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Linn as applied to claim 5 above, and furthering view of Lee.

The rejection is respectfully traversed.

For the reasons discussed above, Linn does not teach all of the elements of the claimed invention. Thus, the Examiner has not presented a *prima facie* case of obviousness. Accordingly, claim 9, which depends from allowable claim 5 and recites features that are neither or disclosed by the prior art, is also allowable.

For the foregoing reasons, reconsideration and allowance of claims 5-15 of the application is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

5. (Once amended) A method for manufacturing a semiconductor device comprising:

forming an insulating layer having a contact hole therethrough on a semiconductor substrate;

forming a diffusion barrier layer on a surface of the insulating layer and on surfaces within the contact hole; and

forming a contact plug in the contact hole by forming a first sub-plug that fills a lower portion of the contact hole and forming a second sub-plug that fills an upper portion of the contact hole on the first sub-plug,

wherein the first sub-plug fills a lower portion of the contact hole to a level substantially below a top surface of the insulating layer.

Claims 13-15 are new.